REMARKS

Favorable reconsideration of this application as presently amended is respectfully requested.

Claims 1-20 are active in this application; Claims 1 and 11 having been amended by way of the present Amendment.

In the outstanding Official Action, Claims 1-20 were rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention; Claims 11, 13, 14, 16, 17, 18 and 20 were rejected under 35 USC §102(b) as being anticipated by Bohan, Jr.; Claims 1-10 were rejected under 35 USC §102(b) as being anticipated by Fisher; and Claims 12, 15 and 19 were indicated as being allowable if rewritten to overcome the rejection under 35 USC §112, second paragraph, set forth in the Office Action and to include all of the limitations of the base claim and any intervening claims.

Applicants acknowledge with appreciation the indication that Claims 12, 15 and 19 include allowable subject matter. However, since Applicants consider that amended Claims 1 and 11 are allowable, Claims 12, 15 and 19 have presently been maintained in dependent form.

In response to the rejection under 35 USC §112, second paragraph, Claims 1 and 11 have been amended to clarify that the frequency of the controlled signal inputted to the gate terminal of the FET is decided in advance, i.e., is predetermined, and that the inductance value of the inductor element is selected in accordance with the predetermined frequency.

If the inductance value is selected in such a way, when the drain voltage of the FET is lower than the source voltage, it is possible to equate the resonance frequency

of the series resonance circuit formed of the reactance component of the impedance between the gate and the source and the inductor element, with the frequency of the controlled signal. If the resonance frequency of the series resonance circuit coincides with the frequency of the controlled signal, such an advantageous effect can be obtained that it is possible to sufficiently reduce the amount of the signal transmitted when the FET is in the off state.

Applicants respectfully traverse the outstanding rejection under 35 USC §102(b) because in Applicants' view, amended Claims 1and 11 patentably distinguish over the cited art for the reasons next discussed.

Firstly addressing the rejection of Claims 11-20 as anticipated by Bohan, in these claims, the series resonance circuit is formed of the reactance component of the impedance between the gate and the source and the inductance element, and the inductance value of the inductor element is selected in accordance with the frequency of the controlled signal. In contrast, the oscillator means 20 of Bohan has the FET 21, and the inductor 28 and the capacitor 26 connected in series between the source terminal of the FET 21 and the ground terminal.

OK w/ draw Bohan

Although an oscillator means 20 is disclosed by Bohan, the inductor 28 of Bohan does not constitute a part of a series resonance circuit, and a series resonance circuit as claimed is neither disclosed nor suggested by Bohan.

Furthermore, in the invention defined by Claims 11-20, the inductance value of the inductor element is selected in accordance with the frequency of the controlled signal inputted to the gate terminal of the FET. However, this claimed feature is neither disclosed nor suggested in Bohan and Bohan does not suggest to set the inductance value of the inductor 28 similarly. Accordingly, Bohan in no way

anticipates or obviates the circuit configuration of claims 11-20, and the outstanding rejection based on Bohan is traversed.

Next, attention is directed to the rejection of Claims 1-10 under 35 USC §102(b) as being anticipated by Fisher. In claims 1-10, the series resonance circuit is also formed of the reactance component of the impedance between the gate and the source, and the inductor element, and the inductance value of the inductor element is selected in accordance with the frequency of the controlled signal. However, Fig. 1 of Fisher discloses the oscillation circuit including the inductor 17 connected between the source terminal of the FET 12 and the ground terminal. In the circuit of Fisher, the controlled signal is not inputted to the gate terminal of the FET 12, and the signal corresponding to the controlled signal is not outputted form the drain terminal of the FET 12.

Furthermore, the inductor of Fisher does not constitute part of a series resonance circuit and Fisher neither discloses nor suggests a series resonance circuit having the same configuration as that of the present invention.

Moreover, in pending Claims 1-10, the inductance value of the inductor element is selected in accordance with the frequency of the controlled signal inputted to the gate terminal of FET. The inductance value of the inductor of Fisher is not adjusted in accordance with the gate signal of the FET 12. Accordingly, Fisher in no way anticipates or obviates the circuit configuration of claims 1-10, and the outstanding rejection based on Fisher is traversed.

Next, it is noted that this amendment is submitted under 37 CFR §1.116 which, after final rejection, permits entry of amendments placing the claims in better form for consideration on appeal. Since the present amendment further clarifies the claimed invention, it is respectfully submitted that the newly submitted claims are in

better form for consideration on appeal. It is therefore respectfully requested that 37 CFR §1.116 be liberally construed and that the present amendment be entered.

Consequently, in view of the present amendment and in light of the above discussion, the pending claims are believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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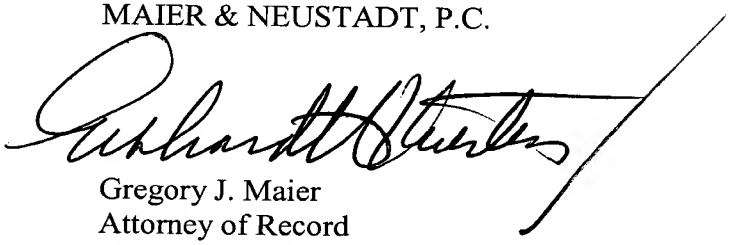

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IN THE CLAIMS:

Please amend claims 1 and 11 as follows.

1. (Twice Amended) A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal with a predetermined frequency and a drain terminal configured to output a signal corresponding to said controlled signal; and

an inductor element provided between a source terminal of said FET and a ground terminal [of said FET], said inductor element having an inductance value selected in accordance with the predetermined frequency of said controlled signal and forming a series resonance circuit with a reactance component of a gate-to-source impedance when a drain voltage of said FET is lower than a source voltage thereof;

wherein when a drain voltage of said FET is lower than a source voltage thereof, a series resonance circuit [it] is formed of [a] the reactance component of [a] the gate-to-source impedance and said inductor element, and [an] the inductance value of said inductor element is set in accordance with [a] said predetermined frequency of said controlled signal.

11. (Twice Amended) A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal with a predetermined frequency and a drain terminal configured to output a signal corresponding to said controlled signal; and

an inductor element and a first capacitor element which are connected to each other in series between a source terminal of said FET and a ground terminal [of said FET], said inductor element having an inductance value selected in accordance with the predetermined frequency of said controlled signal and forming a series resonance circuit with a reactance component of a gate-to-source impedance when a drain voltage of said FET is lower than a source voltage thereof;

wherein when a drain voltage of said FET is lower than a source voltage thereof, [a] the series resonance circuit is formed of [a] the reactance component of [a] the gate-to-source impedance and said inductor element, and [an] the inductance value of said inductor element is set in accordance with [a] the predetermined frequency of said controlled signal.